METHOD AND APPARATUS FOR INCREASING THE DEVICE COUNT ON A SINGLE ATA BUS

Priority is claimed from U.S. Provisional Patent Application No. 60/210,713, filed June 9, 2000 entitled "INCREASING THE DISK DRIVE COUNT ON A SINGLE ATA BUS," which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to increasing the device count on a single ATA bus. In particular, the present invention allows more than two devices to be interconnected to a single channel of an ATA bus.

BACKGROUND OF THE INVENTION

Most personal computers are provided with an Advanced Technology Attachment (ATA) controller for allowing various devices to communicate with the host system using an ATA bus. In a typical system, the ATA controller is provided with two channels, each of which are capable of interconnecting to two devices. In order to increase the number of devices that can be connected to the host system, it is possible to add additional ATA controllers. However, the number of controllers that can be added to any one system is limited, provision of the additional controllers adds to the cost of the system, and providing appropriate cabling is difficult. In addition, such an approach it does not allow for command overlapping between devices and having additional controllers does not improve performance.

As an alternative to an ATA bus for connecting devices to a host system, other bus protocols are available. For instance, the small computer system interface (SCSI) allows as many as 255 devices to be interconnected to a single SCSI bus. However, SCSI

devices are expensive, and an SCSI controller, which is not normally provided as part of a PC type computer, must be used. Furthermore, although the SCSI type bus provides improved performance, the data rate of such a bus cannot be fully exploited by most host systems and devices.

Accordingly, it would be advantageous to provide a low cost method and apparatus to increase the number of devices that can be interconnected to a single channel of an ATA bus. In addition, it would be advantageous to provide such a method and apparatus that was reliable in operation and that offered performance advantages over a standard ATA type interconnection.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method and an apparatus for increasing the drive count on a single ATA type bus are provided. The present invention allows more than two devices to be interconnected to a single ATA type bus. According to the present invention, each device is assigned a unique identifier, and is selected by a selection command provided using the data lines of the ATA type bus.

In accordance with one embodiment of the present invention, a modified ATA type cable having a terminal for interconnecting the cable to a modified ATA controller, and having at least three terminals for interconnecting the modified ATA type cable to at least three modified ATA devices is provided. The controller selects one of the devices by issuing a selection command. Each device interconnected to the ATA type bus receives the selection command, and compares an identifier provided with the selection command to an assigned identifier for that device. The selected device prepares itself to

receive an additional command or data, while those devices that are not selected disconnect themselves from the modified ATA type bus.

According to another embodiment of the present invention, each device to be interconnected to a modified ATA type controller is provided with a different identifier. In operation, the controller issues a selection command that includes an identifier corresponding to one of the assigned identifiers. In response to receiving the selection command, the selected device prepares to receive an additional command or data, while those devices that were not selected disconnect themselves from the modified ATA bus.

According to an embodiment of the present invention, as many as 256 devices may be interconnected to a single modified ATA type channel. According to another embodiment of the present invention, as many as eight devices may be interconnected to a single channel of a modified ATA type bus.

In accordance with still another embodiment of the present invention, a device suitable for use in connection with the present invention includes a standard ATA type device that has been modified to compare a received identifier to an assigned identifier in response to receiving a selection command. A controller suitable for use in connection with the present invention may be an ATA type controller modified to issue a selection command using data lines provided as part of the ATA bus. A cable or interconnection suitable for use in connection with the present invention may be an ATA cable modified to allow more than two devices to be interconnected to the modified ATA type controller.

Based on the foregoing summary, a number of salient features of the present invention are readily discerned. A method and an apparatus for increasing the device

count of a single ATA type bus are provided. In particular, the method and apparatus of the present invention allow more than two devices to be interconnected to a single modified ATA bus. In addition, the method and apparatus of the present invention allow the interconnection of more than two devices to a single ATA channel with only slight modifications to the operating parameters of an ATA controller and ATA type device, and with the provision of an ATA type cable, modified to provide terminals for the desired number of devices.

Additional advantages of the present invention will become readily apparent from the following discussion, particularly when taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating a system utilizing a modified ATA bus in accordance with the present invention;

Fig. 2 is a flowchart illustrating the operational steps taken during power up of an embodiment of the present invention;

Fig. 3 is a flowchart illustrating operational steps taken in response to a device selection command in accordance with an embodiment of the present invention;

Fig. 4 is a flowchart illustrating operational steps taken during device selection in accordance with an embodiment of the present invention;

Fig. 5 is a block diagram illustrating hardware suitable for use in connection with an embodiment of the present invention;

Fig. 6 is a flowchart illustrating operational steps taken during power up of yet

another embodiment of the present invention; and

Fig. 7 is a flowchart illustrating operational steps taken during drive selection in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION

Fig. 1 illustrates in block diagram form a system **100** utilizing a modified ATA bus system **104** having an increased device count in accordance with an embodiment of the present invention. In addition to the modified ATA bus system **104**, the system **100** includes a host computer **106**. The host computer **106** generally includes a system bus **108**, a processor **112**, and system memory **116.**

The modified ATA bus system **104** generally includes a modified ATA interface or controller **120**, a modified ATA bus **124** and a plurality of modified ATA devices **128a, 128b, 128c, 128d, 128e, 128f, 128g**, and **128h**. In general, the components of the modified ATA bus system **104** in accordance with the present invention are altered as compared to the components used in connection with a conventional ATA bus as described in detail below.

The modified ATA interface or controller **120** generally serves to interconnect the system bus **108** to the various devices **128** via the modified ATA bus **124.** In general, the modified ATA controller **120** translates between the protocol of the system bus **108** and the protocol of the ATA bus (or input/output bus) **124.** In a typical ATA controller, no more than two devices may be interconnect to each of the provided first and second channels. However, the controller **120** of the present invention is capable of having more than two devices **128** interconnected to a single channel. Briefly stated, the firmware of

the controller **120** of the present invention is modified from a controller in accordance with a conventional ATA bus in that the controller **120** of the present invention is capable of sending a selection command over data lines provided as part of the ATA bus **124** prior to issuance of a command or data directed to the selected device **128.**

The modified ATA bus **124** of the present invention is, according to one embodiment of the present invention, identical to a conventional ATA bus, in that the modified ATA bus **124** includes an 8 bit data bus, and signal lines for each of the DASP, PDIAG and IRQ signals. In addition, the conductors used to provide above-mentioned data bus and signal lines are terminated in connectors provided in accordance with the ATA protocol. However, unlike a conventional ATA bus, the modified ATA bus **124** of the present invention may be provided with more than two terminals to which devices **128** may be interconnected. According to one embodiment of the present invention, the modified ATA bus **124** is provided with terminals for interconnecting as many as eight devices **128** to the bus **124** and in turn to the controller **120.** According to another embodiment of the present invention, a modified ATA bus **124** having decoding logic may receive individual DASP, PDIAG and IRQ signals and may feed those signals to registers in the controller **120**, as will be explained in greater detail below.

According to still another embodiment of the present invention, as many as 256 terminals may be provided on the modified ATA bus **124** for interconnecting as many as 256 devices **128** to the modified ATA bus **124** and in turn to the controller **120.** However, alterations to standard ATA hardware and signalling protocols would be required in order to operably interconnect such a large number of devices to a controller

120.

Briefly stated, the devices **128** are modified as compared to a conventional ATA type device in that they are each assigned a different identifier, and in that they are adapted to compare a identifier received as part of a selection command to the assigned identifier. In a typical implementation, these modifications from a typical ATA device may be accomplished by modifying the firmware of the device **128.** For example, the device **128** may be provided with a processor having firmware running thereon that includes instructions for comparing the received identifier to the assigned identifier. Furthermore, the firmware may be configured such that a device **128** is disconnected from the modified ATA bus **124** if it is not selected. If a device **128** is selected, the firmware may cause a confirmation signal to be passed from that device to the controller **120** over the modified ATA bus **124.**

In the embodiment illustrated in **Fig. 1**, eight devices **128a-128h** are shown. Accordingly, the modified ATA bus system **104** illustrated in **Fig. 1** may be configured as a system **104** to which as many as eight devices **128** may be operatively interconnected to a single channel of the controller **120.** Alternatively, the embodiment illustrated in **Fig. 1** could be one in which as many as 256 devices **128** may be connected, but that has only eight devices **128** installed. As can be appreciated by one of skill in the art, by selectively asserting one bit of an eight bit selection command or word, a particular device **128** from a group of eight such devices **128** may be selected. Furthermore, it can be appreciated that one device **128** from among 256 devices **128** may be selected using a binary number defined by an eight bit identifier or selection command. Accordingly, using an 8 bit bus,

a command sent over such a bus using an 8 bit identifier may select from among 256 devices **128**.

The devices **128** may include any device capable of communicating across an ATA bus that has been modified as described herein **124.** In a typical implementation, the devices **128** include storage devices. For example, the devices **128** may include hard disk drives, floppy disk drives, optical drives and tape drives.

The devices **128** are each assigned a different identifier. The identifier may be assigned through hardware or software. For example, jumpers provided on an exterior of each device **128** may be used to assign an identifier to the devices **128**. Alternatively, an identifier may be assigned by setting software switches during initialization of the devices **128.**

With reference to **Fig. 2**, steps taken to power up a modified ATA system **104** in accordance with an embodiment of the present invention are illustrated. Initially, at step **200**, the power is turned on. At step **204**, devices **128** that are not logical unit zero (*i.e.* that are not designated as a master) configure their databus drivers and drivers for the INTRQ and PDIAG signal lines to a high impedance condition. The drive that has been assigned logical unit zero then configures its PDIAG driver to a high impedance condition (step **208**).

At step **212**, a determination is made as to whether the PDIAG signal line provided as part of the ATA bus **124** has been negated. If it has not been negated, the system waits at step **212.** If the PDIAG signal line has been negated, (i.e., all of the devices **128** attached to the bus **124** have configured their driver for the PDIAG signal

line in a high impedance condition) the system proceeds to step **216.** At step **216**, the device **128** that is logical unit zero asserts the PDIAG signal on the bus **124**. The device that is logical unit zero also negates the BSY bit, and asserts DRDY bit in the status register of the device **128.** At step **220**, a determination is made as to whether the BSY bit is negated and the DRDY bit asserted. If this condition is not met, the modified ATA bus system **104** waits until the condition is satisfied. Once the condition is satisfied, power up of the modified ATA bus system **104** is complete **224.**

With reference now to **Fig. 3**, a flowchart illustrating the response of a device to a selection command in accordance with an embodiment of the present invention is illustrated. Initially, at step **300**, a device selection command is received on the data bus of the modified ATA bus **124.** At step **304**, each device **128** determines whether its identifier matches the identifier transmitted as part of the drive selection command. If a device **128** determines that there is a match, the selected device **128** determines whether the modified ATA bus system **104** is using hardware registers (step **308**). That is, the selected device **128** determines whether registers such as may be provided as part of the controller **120** are being utilized for conveying certain information regarding the modified ATA bus system **104.** If the modified ATA bus system **104** is being used in connection with hardware registers, the selected device **128** enables its databus (step **312**) and asserts the DASP signal (step **316**).

If the modified ATA bus system **104** is not configured for use with hardware registers, the selected device **128** configures its PDIAG signal line driver in a high impedance condition (step **320**). At step **324**, the selected device **128** determines whether

the PDIAG signal line has been negated. The selected device **128** idles at step **324** until the PDIAG signal line has been negated.

Once the PDIAG signal line has been negated, the selected device **128** asserts the PDIAG signal (step **328**). In addition, the selected device **128** enables its databus and INTRQ drivers (step **332**) and asserts the INTRQ signal (step **336**).

If a device **128** determines at step **304** that the identifier assigned to that device **128** does not match the identifier specified as part of the selection command, the device **128** proceeds to step **340.** In step **340**, the device **128** determines whether the modified ATA bus system **104** includes hardware registers. If the modified ATA bus system **104** uses hardware registers, the device **128** configures its data bus drivers such that they present a high impedance to the data bus (step **344**) and the device **128** negates the DASP signal line (step **348**). If the modified ATA bus system **104** is not configured for use with hardware registers, the device **128** configures its databus drivers, its INTRQ and its PDIAG drivers such that they present a high impedance to the respective data or signal lines (step **352**).

With reference now to **Fig. 4**, a flowchart illustrating the selection of a device **128** in connection with a modified ATA bus system **104** in accordance with the present invention that does not utilize hardware in addition to that normally supplied with a conventional ATA bus is illustrated. Initially, at step **400**, the host system **106** issues a device selection command to select a one of the devices **128** (device n). The device selection command is issued through the controller **120.** The devices **128** all receive the selection command over the data bus of the bus or channel **124** of the modified ATA

system **104** (step **404**). The devices **128** that are not selected (i.e., whose identifiers do not match the identifier transmitting as part of the selection command) configure their data bus drivers and INTRQ drivers such that they present a high impedance to the modified ATA bus **124** (step **408**). In addition, the devices **128** that are not selected negate the PDIAG signal line (step **408**).

The selected device **128** presents a high impedance at that devices' interconnection to the PDIAG signal line (step **412**). As noted above, the selected device **128** is that device having an assigned identifier matching the identifier transmitted with the selection command. At step **416**, the selected device **128** determines whether the PDIAG signal line is negated (step **416**). If it is not, the selected device **128** idles at step **416.** If the PDIAG signal line is negated, the selected device asserts the PDIAG signal, and enables its databus and INTRQ drivers (step **420**). The selected device also asserts the INTRQ signal (step **424**).

At step **428**, the controller **120** determines whether the INTRQ signal has been asserted. If yes, the system host **106**, through the controller **120**, reads the status register in the selected device **128** to verify the successful selection of the device **128** (step **432**). The host system **106** may then issue additional commands, such as commands to send or receive data, to the selected device **128** through the controller **120** (step **436**). Following a command to send or receive data, data may be passed between the controller **120** and the selected device **128**.

With reference now to **Fig. 5**, additional hardware that may be provided in connection with a modified ATA bus system **104** in accordance with the present

invention is illustrated in block diagram form. Shown in **Fig. 5** are the modified ATA bus **124** and various control registers **500.** In addition, **Fig. 5** shows an AND gate **504**, an OR gate **508**, and interrupt request signal line **512.**

The control registers **500** generally include a selected status register **516**, a ready status register **520**, an interrupt pending register **524**, and an interrupt mask **528.** As will be appreciated by those of skill in the art, the various control registers **500** may be accessed through the register access address (control block register 4) and register access data (control block register 5) available as part of a conventional ATA controller. Furthermore, it will be appreciated that the AND gate **504**, OR gate **508** and interrupt request signal line **512** represent hardware that is not found in connection with a conventional ATA system, and that is unique to the modified ATA bus system **104** of the present invention.

Fig. 5 illustrates as an input to the selected status register **516** the DASP signal bus **532.** Accordingly, the DASP pin of each device **128** of the modified ATA system **104** may selectively drive a corresponding DASP signal line on the DASP signal bus **532** to set a bit in the selected status register **516.**

The input to the ready status register **520** is the PDIAG signal bus **536.** Each device **128** included in the modified ATA bus system **104** may selectively drive the individual PDIAG signal line associated with that device **128**. Accordingly, each device **128** is individually interconnected to the ready status register **520** by a dedicated signal line on the PDIAG signal bus **536** such that each device may selectively set a bit in the ready status register **520.**

The input to the interrupt pending register **524** is the IRQ signal bus **540.** Each device **128** may selectively drive the individual IRQ signal line associated with it. Accordingly, the IRQ signal bus **540** provides an individual IRQ signal line for each device **128** included in the modified ATA system **104.** The IRQ signal bus **540** is also interconnected to the AND gate **504**, as will be described in greater detail below. Therefore, each device **128** may selectively set a bit in the interrupt pending register **524.**

As can be appreciated by one of skill in the art, the DASP signal bus **532**, the PDIAG signal bus **536**, and the IRQ signal bus **540** shown in **Fig. 5** are 8 bit busses provided as part of the modified ATA bus **124**, as is the data bus **502.** Decode logic to set the appropriate bit or bits in the registers **500** may be included as part of the hardware used to implement the modified ATA bus **124** of such an embodiment of the present invention. The decode logic may be provided using one or more field programmable gate arrays. Furthermore, it can be appreciated that if more than eight devices are to be supported by the modified ATA system **104**, alterations to the way in which the devices **128** drive the lines of the signal buses **532**, **536** and **540** must be made. For example, each device **128** may be provided with an eight bit driver for each of the DASP, PDIAG, and IRQ signals, and may be interconnected to each of the data lines in the DASP **532**, PDIAG **536**, and IRQ **540** buses. As many as 256 devices **128** could then be connected to the modified ATA bus system **104,** provided that enough terminals are also provided for interconnecting the devices **128** to the modified ATA bus **124.** Alternatively, an individual signal line for each of the provided devices **128** must be provided by each of the DASP **532**, PDIAG **536**, and IRQ **540** signal buses, and a corresponding bit provided

in the registers **500**. As many devices as signal lines and register bits were provided could then be connected to the modified ATA system **104**, provided that a like number of terminals were provided by the modified ATA bus **124**, and provided that alterations were made to the hardware and/or signalling protocols to accommodate increased signal path lengths.

The interrupt mask register **528** is written by the controller **120.** As can be appreciated, typically only one bit of the interrupt mask register **528** will be enabled. A mask register bus **544** provides a signal indicative of the enabled bits in the interrupt mask register **528** to the AND gate **504.** The AND gate **504** is also provided with the signals from the IRQ signal bus **540.** In a system **104** having as many as eight devices **128** interconnected thereto, both the IRQ signal bus **540** and the interrupt mask register bus **544** will be eight bits wide. Accordingly, the AND gate **504** will typically consist of eight two input AND gates. The interrupt logic bus **548** provides the output from the AND gate **504** to the OR gate **508.** If any one bit of the interrupt mask register **528** matches any one IRQ signal on the IRQ signal bus **540**, at least one of the bits on the interrupt logic bus **548** will be high, and the output from the OR gate **508** will also be high. A high signal from the OR gate **508** indicates that at least one selected device **128,** as confirmed by the selection stored in the interrupt mask register **528,** is generating an interrupt request. Such request is provided to the host **106** over the interrupt signal line **512.**

In general, the use of additional hardware as illustrated in **Fig. 5** allows the modified ATA bus system **104** to manage interrupt requests from the devices **128.** In

addition, the embodiment of the present invention illustrated in **Fig. 5** provides the opportunity for overlapping commands across drives. For instance, commands can be overlapped by issuing a drive command to a first drive and before the commanded operation is completed issuing a second command to a second drive.

In an embodiment in which additional hardware such as that illustrated in **Fig. 5** is provided, the modified ATA bus **104** may operate according to a different protocol. With reference now to **Fig. 6**, the operation of an embodiment employing one such alternative protocol is illustrated in block diagram form. Initially, at step **600**, the power to the modified ATA bus system **104** is turned on. Within a selected amount of time, for example from about 1-10 milliseconds, each device **128** interconnected to the modified ATA bus system **104** asserts its associated DASP signal line (step **604**). At step **608**, each device **128** asserts its PDIAG signal line, and negates its DASP signal line when the device **128** is ready to receive a command.

At step **612**, the controller **120** determines whether all of the devices **128** have negated the DASP signal. If no, the controller **120** waits until all devices **128** have negated their DASP signal line (step **612**). The controller **120** next determines whether all of the devices **128** have asserted PDIAG (step **616**). If they have not, the controller **120** may notify the host system **106** of a problem or that fewer than the expected or possible number of devices **128** are connected, or wait until the devices **128** have all asserted PDIAG. After all of the devices **128** have asserted PDIAG, or after the controller **120** has been instructed or has decided to continue with less than all of the devices **128** asserting PDIAG, the host **106** may read or write to the modified ATA bus **104** through

the controller **120** (step **620**).

With reference now to **Fig. 7**, the selection of a device **128** in accordance with an embodiment of the present invention utilizing the hardware illustrated in **Fig. 5** is shown. Initially, at step **700**, the host system **106** issues a first or device selection command to select a device (device n) (step **700**). The devices **128** receive the device selection command over the data lines **502** of the modified ATA bus **124** (step **704**). The devices that are not selected configure their databus drivers to present a high impedance to the data bus **502**, and configure their DASP driver so as to negate the DASP signal corresponding to that device **128** (step **708**).

A selected device **128** enables its databus **502** drivers, and asserts its DASP signal (step **712**). At step **716**, the controller **120** determines whether only the intended device **128** is indicated as selected in the selected status register **516.** Once the controller **120** has confirmed that only the selected device **128** is indicated as selected, the host system **106** may issue a second command, for example a command to read or write data to the selected device **128** through the controller **120** and over the modified ATA bus **124** (step **720**).

From the foregoing discussion, it can be appreciated that the cabling used to implement the modified ATA bus **124** of the present invention is similar to that of a conventional ATA buses cabling. Indeed, in an embodiment without the hardware illustrated in **Fig. 5** that is in addition to that provided as part of a conventional ATA system, and to which no more than two devices **128** are to be attached, the cable implementing the modified ATA bus **124** may be identical to a conventional ATA bus

cable. In order to connect additional drives to the modified ATA bus system **104**, the cable of the modified ATA bus **124** need only be provided with additional *terminals to* allow the physical interconnection of such additional devices **128.**

In accordance with one embodiment of the present invention, and in particular one that employs additional hardware such as is illustrated in **Fig. 5**, a back plane for implementing the physical channel of the modified ATA bus **124** is provided. In particular, the back plane is adapted to minimize the distance that signals must travel between the controller **120** and any of the attached devices **128.** In accordance with one embodiment of the present invention, the back plane is adapted to minimize capacitance in the signal lines between the controller **120** and the attached devices **128.** A framework for holding multiple devices **128** in close proximity to one another may therefore be beneficially provided in connection with an embodiment of the present invention. For example, a framework for holding eight hard disk drives (i.e., eight devices **128**) having integrated connectors to allow each of the hard disk drives to be interconnected to the modified ATA bus **124** in a modular fashion may be provided. In accordance with one embodiment of the present invention, the framework is no taller than necessary in order to accommodate the eight hard disk drives. For example, the framework may result in a drive stack height of 8 ½ inches. The back plane may also incorporate the DASP **532,** PDIAG **536** and IRQ **540** signal busses, decode logic associated with those busses **532, 536** and **540**, and components **504, 508, 512** and **548** for interrupt management that are in addition to or modified from components provided as part of a conventional ATA bus

The foregoing discussion of the invention has been presented for purposes of

illustration and description. Further, the description is not intended to limit the invention to the form disclosed herein. Consequently, variations and modifications commensurate with the above teachings, within the skill and knowledge of the relevant art, are within the scope of the present invention. The embodiments described herein are further intended to explain the best way presently known of practicing the invention and to enable others skilled in the art to utilize the invention in such or in other embodiments or with various modifications required by their particular application or use of the invention. It is intended that the appended claims be construed to include the alternative embodiments to the extent permitted by the prior art.